Amendment to the claims:

11. (Currently Amended) An information processing unit,

~~adding instruction codes which are different from each other in the same group of instruction to each instruction, and sorting the instructions executable into a plurality of groups of instructions,~~

comprising a decoder circuit selecting an instruction ~~the~~ group ~~of instruction~~ corresponding to ~~the~~ an inputted instruction code ~~inputted thereto~~, based on a ~~input~~ history of the inputted instruction code, and uniquely ~~to determine the~~ an instruction to be executed selected from a plurality of executable instructions in accordance with the inputted ~~uniquely by the~~ instruction code ~~inputted thereto~~, and

wherein said plurality of executable instructions are sorted into a plurality of instruction ~~setting a prescribed instruction code, which assigns an optional instruction depending on the other~~ groups ~~of~~ and each instruction is given with ~~, to each group of instructions, and wherein said decoder circuit controls to execute the~~ an instruction ~~which is assigned to said prescribed instruction~~ code[[,]] different from others within the same instruction group in advance, each instruction group having a certain instruction code to which an instruction belonging to another instruction group can be assigned, and said decoder circuit outputting a control signal corresponding to the instruction assigned to the certain ~~when said prescribed~~ instruction code to a processor element, when said certain instruction code is inputted.

12. (Currently Amended) The information processing unit according to claim 11, wherein ~~said~~ the instruction, which belongs to another ~~depending on the other group of~~ instruction~~, which~~ group and is assigned to ~~said prescribed~~ the certain instruction code, ~~can be~~ is changeable ~~changed~~.

13. (Currently Amended) The information processing unit according to claim 11, wherein ~~a plurality of said prescribed~~ each of the instruction groups has a plurality of the certain instruction codes[[,]] to which an instruction belonging to the other instruction

~~assign optional instructions depending on the other~~ group can be assigned. ~~of instruction, are provided to groups of the instruction.~~

14. (Currently Amended) An information processing unit, comprising:

~~adding instruction codes which are different from each other in the same group of instruction to each instruction, and sorting the instructions executable into a plurality of groups of instructions, and~~

~~comprising~~ a decoder circuit retaining information corresponding to a history of inputted instruction codes, selecting an instruction group corresponding to an inputted ~~holding a prescribed information corresponding to input history of the instruction codes, selecting the group of the instruction corresponding to the~~ instruction code ~~inputted thereto,~~ based on the information, and uniquely determining an instruction to be executed selected from a plurality of executable instruction in accordance with the inputted ~~said prescribed information, to determine the instruction to be executed uniquely by the~~ instruction code, and ~~inputted thereto,~~

wherein said plurality of executable instructions are sorted into a plurality of instruction groups and each instruction is given with an ~~decoder circuit changes said prescribed information temporary, when a prescribed~~ instruction code different from other instruction codes within the same instruction group in advance, and said decoder circuit temporarily changes the information when a certain instruction code is inputted.

15. (Currently Amended) The information processing unit according to claim 14, wherein said decoder circuit determines an instruction to be executed ~~the~~ based on the inputted instruction code only irrespective of the ~~to be executed, regardless of said prescribed~~ information corresponding to the ~~input~~ history of ~~the~~ instruction codes, when an instruction code, ~~for determining the~~ in which an instruction to be executed in accordance with ~~uniquely by only~~ the instruction code only is uniquely determined, is inputted ~~thereto is inputted~~.

16. (Currently Amended) An information processing unit executing an instruction ~~which is~~ determined in accordance with an inputted ~~by an~~ instruction code, ~~inputted thereto~~, comprising:

a decoder circuit ~~holding a prescribed~~ retaining information corresponding to an input history of a plurality of inputted instruction codes ~~inputted thereto~~, and uniquely determining ~~the~~ an instruction to be executed selected from plurality of ~~uniquely, based on the~~ instructions assigned to the ~~code~~ inputted ~~thereto as well as the prescribed information, from a plurality of instructions which are assigned to the said~~ instruction code in accordance with a combination of the information and the inputted instruction code ~~thereto~~.

17. (Currently Amended) The information processing unit according to claim 16, wherein said decoder circuit determines an instruction to be executed selected from a plurality of ~~the~~ executable instructions, and said plurality of executable ~~are sorted into a plurality of groups of instructions and the~~ instructions are sorted into a plurality of instruction groups and ~~codes which are different from~~ each instruction is given with an instruction code different from others within ~~in~~ the same instruction group in advance ~~are added to each instruction~~.

18. (Currently Amended) The information processing unit according to claim 16, wherein said decoder circuit determines an ~~the~~ instruction to be executed, based on the inputted instruction code only, irrespective of the ~~regardless of said prescribed~~ information corresponding to the history of inputted ~~input history of the~~ instruction codes, when an instruction code, in which an instruction to ~~for determining the instruction to~~ be executed in accordance with ~~uniquely by only~~ the instruction code only is uniquely determined, ~~inputted thereto~~ is inputted.

19. (Currently Amended) An information processing unit, comprising:

a plurality of processors on one chip each capable of executing ~~which execute~~ instructions independently ~~in one chip~~, and

wherein ~~the instructions executable by said processor are sorted into a plurality of groups of instructions indicated by a group code, with the instruction codes which are different from each other in the same group of instruction being added to each instruction, and wherein said each processor comprises a decoder circuit which determines~~ each of said processors comprises:

a decoder circuit uniquely determining an instruction to be executed ~~uniquely~~ selected from a plurality of executable instructions based on an inputted instruction code and a group code corresponding to ~~input~~ a history of the inputted instruction codes; and

a processor element ~~which executes~~ executing an operation corresponding to a control signal ~~supplied~~ provided from said decoder circuit, and ~~wherein the instruction executable by said processor~~

wherein said plurality of executable instructions are sorted into a plurality of instruction groups assigned by the group code and each instruction is given with an instruction code different from others within the same instruction group in advance, and the executable instruction includes an alias instruction ~~which assigns in advance the optional instruction for the~~ to which an instruction belonging to the other instruction group can be assigned in advance to an internal instruction code ~~generated by~~ constituted by the group code and the ~~input~~ inputted instruction code.

20. (Currently Amended) The information processing unit according to claim 19, wherein ~~said~~ each ~~processor~~ of said processors further comprises a group register ~~which stores~~ storing the group ~~codes set on the basis of the input~~ code, which is set up based on the history of ~~said~~ the inputted instruction code.

21. (Currently Amended) The information processing unit according to claim 20, wherein ~~said~~ each ~~processors~~ of said processors further comprises a ~~look up~~ lookup table ~~which defines the rule for changing~~ prescribing a change in a rule of the group code stored in said group register.

22. (Currently Amended) The information processing unit according to claim 21, wherein said ~~look up~~ lookup table ~~defines~~ is set up with a combination of ~~an~~ an instruction mask for setting a mask bit ~~to be masked~~, an instruction code for comparing the ~~instruction with the~~

internal instruction code ~~generated by the group code and the input instruction code, and~~ , and the changed group code.

23. (New) The information processing unit according to claim 11, wherein each instruction group is given with a group code different from others in the instruction group in advance, and the group code corresponding to the inputted instruction code is determined based on the history of the inputted instruction code.

24. (New) The information processing unit according to claim 14, wherein the information corresponding to the history of inputted instruction codes is a group code for selecting said instruction group.

25. (New) The information processing unit according to claim 17, wherein said information corresponding to the history of inputted instruction codes is a group code for selecting said instruction group.